$R_{DS(on),typ}$ V_{GS}=4.5V

13 A

Conditions		Unit
		A
		V
		V
-	120	A
L=0.1mH, T_C	31	mJ
	3.1	W

Absolute Maximum Ratings

75

July. 2021

Electrical Characteristics at T_j ! a b bb "

Static Characteristics

Parameter	Symbol	Conditions	Value min	Value typ	Value	Unit
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=250 A	100		-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=250 A	1.4	2.0	2.4	
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS}=0V, V_{DS}=100V, T_j	-	-	1	A
		V_{GS}=0V, V_{DS}=100V, T_j	-	-	100	
Gate to Source Leakage Current	I_{GSS}	V_{GS} $_{DS}$=0V	-	-	100	nA
Drain to Source on Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=20A	-		9.8	m
		V_{GS}=4.5V, I_D=20A	-	11	13	
Transconductance	g_{fs}	V_{DS}=5V, I_D=20A	-	85	-	S
Gate Resistance	R_G	V_{GS}=0V, V_{DS} Open, f=1MHz	-	2.2	-	

Dynamic Characteristics

Input Capacitance	C_{iss}		-	1622	-	
Output Capacitance	C_{oss}	V_{GS}=0V, V_{DS}=50V, f=1MHz	-	538	-	pF
Reverse Transfer Capacitance	C_{rss}		-	8.9	-	
Total Gate Charge	Q_g(10V)		-	26	-	
Total Gate Charge	Q_g(4.5V)	V_{DD}=50V, I_D=20A, V_{GS}=10V	-	13	-	nC
Gate to Source Charge	Q_{gs}		-	5	-	
Gate to Drain (Miller) Charge	Q_{gd}		-	6	-	
Turn on Delay Time	$t_{d(on)}$		-	13	-	
Rise time	t_r	V_{DD}=50V, I_D=20A, V_{GS}=10V,	-	6	-	ns
Turn off Delay Time	$t_{d(off)}$	R_G=10 ,	-	24	-	
Fall Time	t_f		-	5	-	

Reverse Diode Characteristics

Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_F=20A	-	0.9	1.2	V
Reverse Recovery Time	t_{rr}	V_R=50V, I_F=20A, dI_F/dt=500A/ s	-	30	-	ns
Reverse Recovery Charge	Q_{rr}		-	103	-	nC

Fig 1. Typical Output Characteristics

Figure 2. On-Resistance vs. Gate-Source Voltage

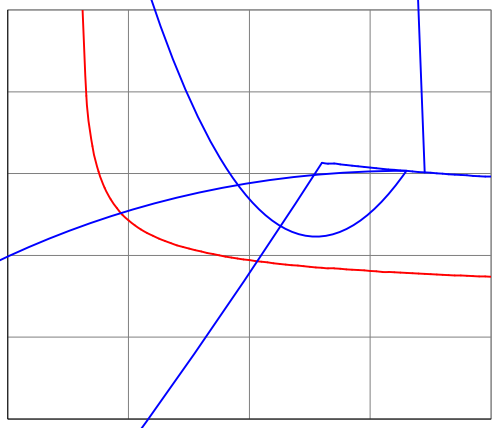


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

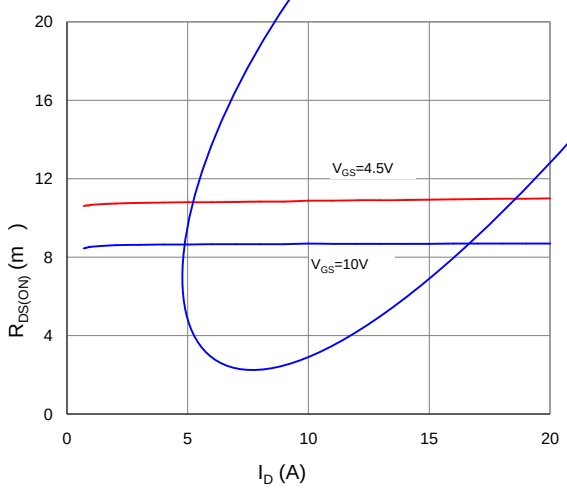


Figure 4. Normalized On-Resistance vs. Junction Temperature

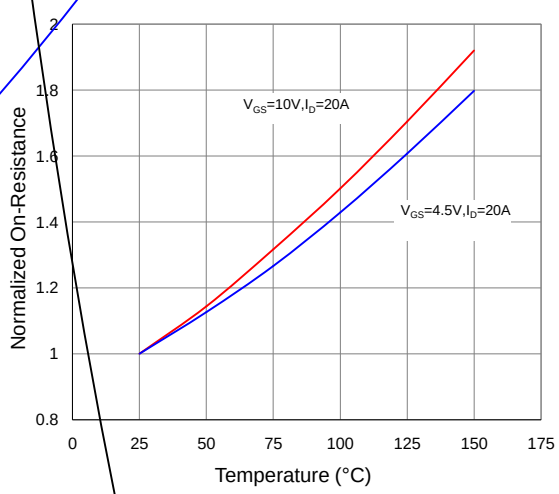


Figure 5. Typical Transfer Characteristics

Figure 6. Typical Source-Drain Diode Forward Voltage

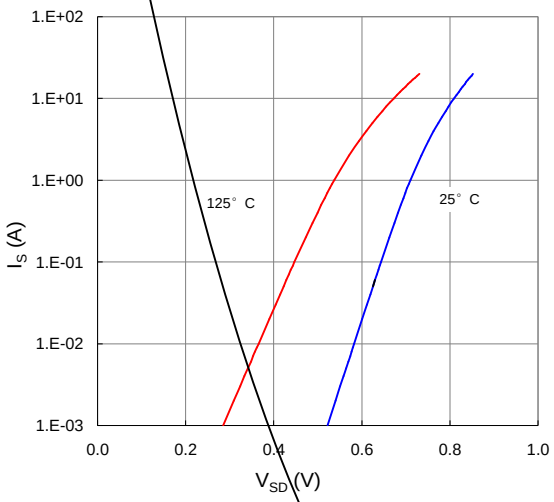


Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

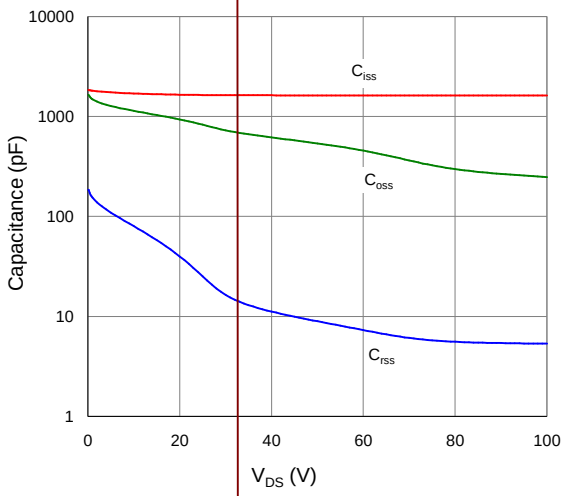


Figure 9. Maximum Safe Operating Area

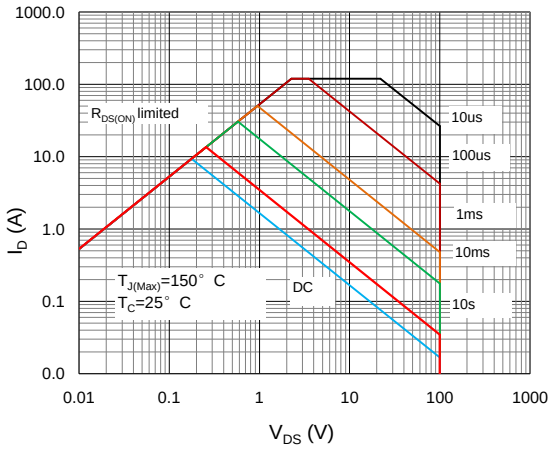


Figure 10. Maximun Drain Current vs. Case Temperature

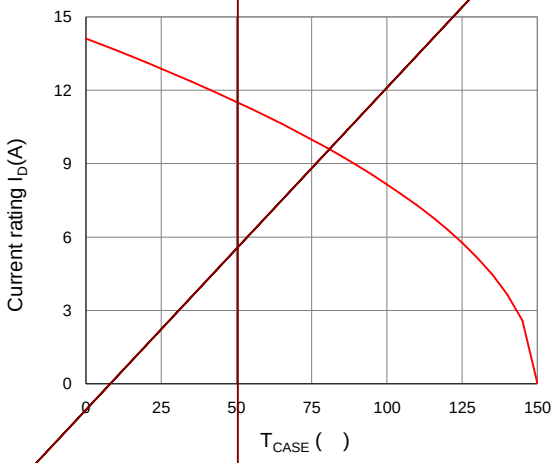
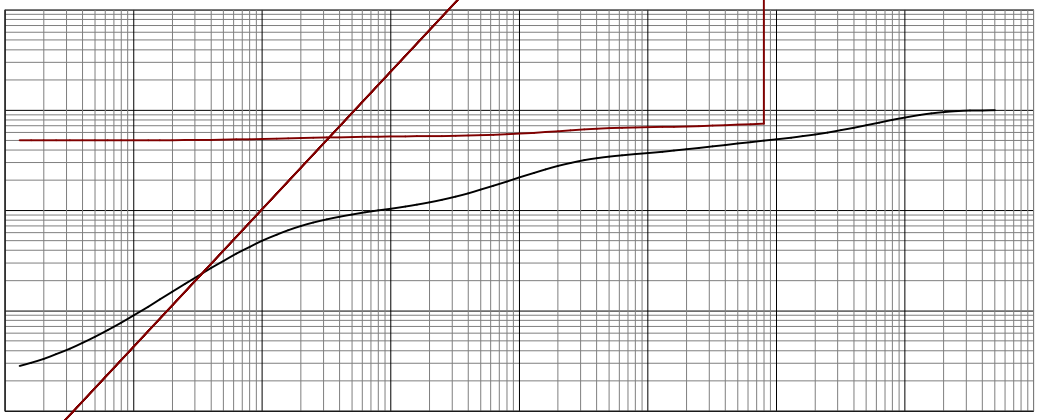
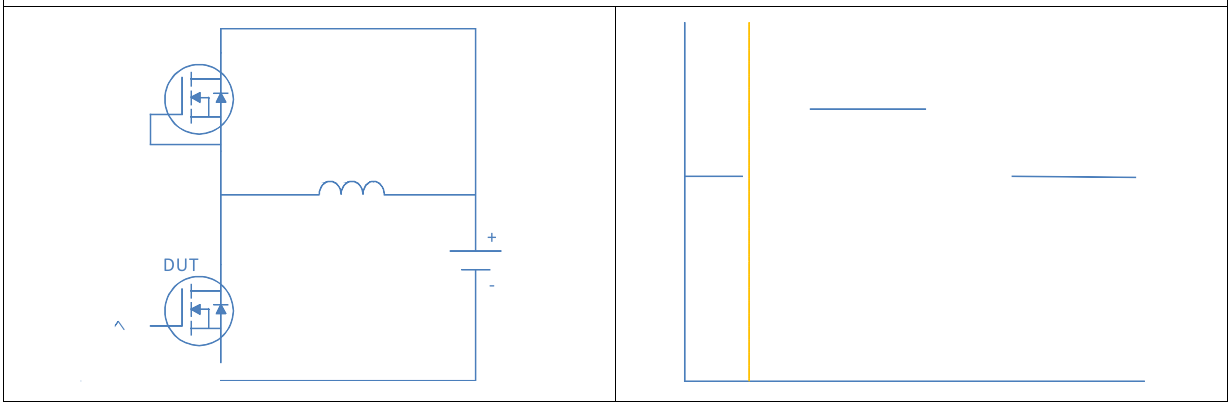


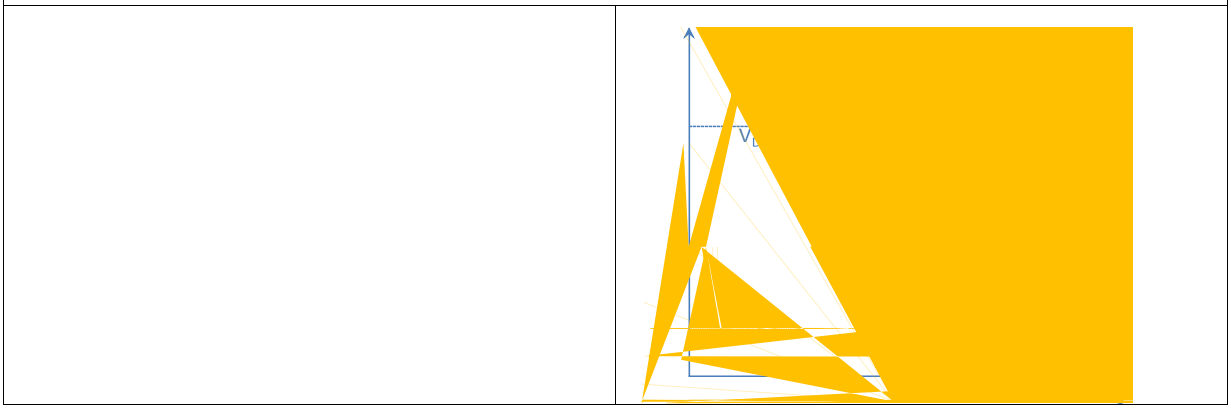
Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Case



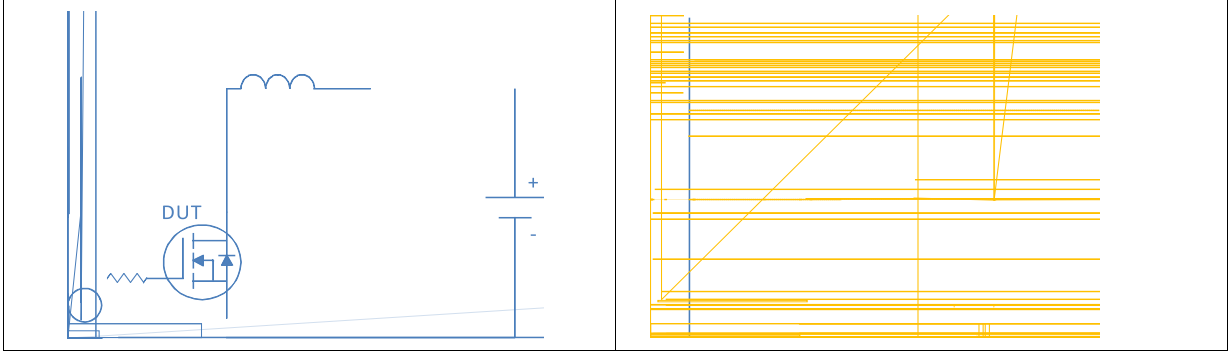
Inductive switching Test



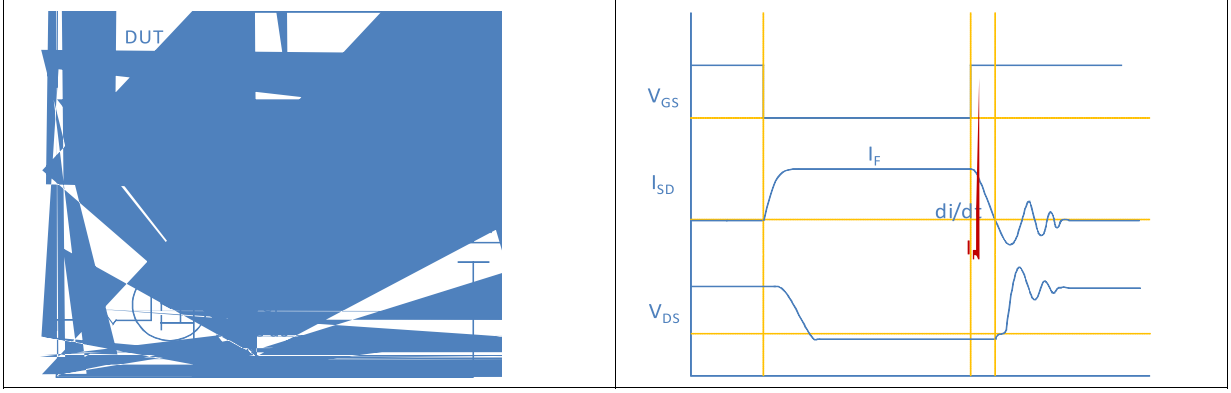
Gate Charge Test



Uclamped Inductive Switching (UIS) Test

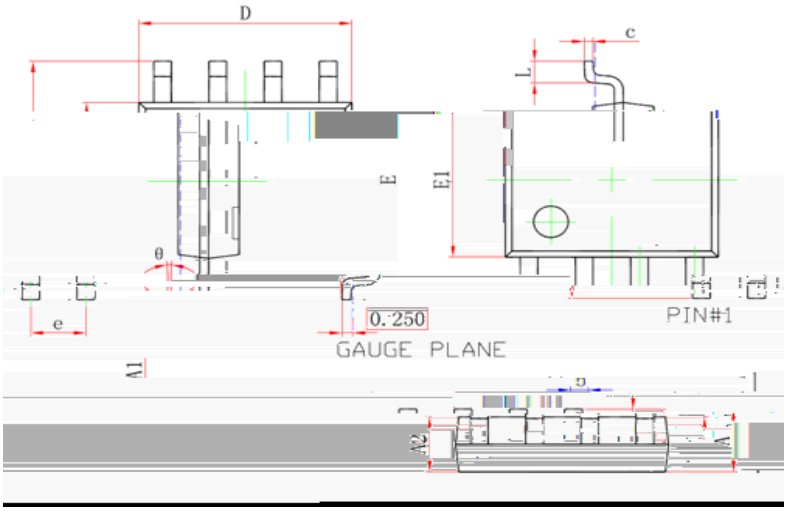


Diode Recovery Test



Package Outline

SOIC-8, 8 leads



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.250	1.650	0.049	0.065
b	0.310	0.510	0.012	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 (BSC)		0.050 (SBC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.031
θ	0°	8°	0°	8°